SanDisk MultiMediaCard Technical Reference

Application Note

Version 1.0

Document No. 80-36-00282

October 2003

SanDisk Corporation

Corporate Headquarters • 140 Caspian Court • Sunnyvale, CA 94089

Phone (408) 542-0500 • Fax (408) 542-0503

www.sandisk.com

SanDisk® Corporation general policy does not recommend the use of its products in life support applications where in a failure or malfunction of the product may directly threaten life or injury. Per SanDisk Terms and Conditions of Sale, the user of SanDisk products in life support applications assumes all risk of such use and indemnifies SanDisk against all damages.

The information in this document is subject to change without notice.
SanDisk Corporation shall not be liable for technical or editorial errors or omissions contained herein; nor for incidental or consequential damages resulting from the furnishing, performance, or use of this material.

SanDisk products are covered or licensed under one or more of the following U.S. Patent Nos. 5,070,032; 5,095,344; 5,168,465; 5,172,338; 5,198,380; 5,200,959; 5,268,318; 5,268,870; 5,272,669; 5,418,752; 5,602,987. Other U.S. and foreign patents awarded and pending.

Lit. No. 80-36-00282 Rev. 1.0, Edited on 10/10/03

Printed in U.S.A.

Revision History

- *Revision 1.0—Reprint of Initial release as MMC Q&As*

Introduction

This application note provides users with answers to frequently asked questions about SanDisk MultiMediaCard (MMC) parameters.

Q & A

►What is the difference between MMC terms and functions Idle, Inactive, Standby, and Sleep?

Idle, Inactive and Standby are basically *protocol states* and **not** *electrical* states. Each of these states is described in Figure 5-1 of section 5.2 of the *MultiMediaCard Product Manual.* All of these states, except for Sleep, have no meaning in SPI mode.

State	Description
Idle	Entered from Command 0 and remains until a valid Command 1 response. MMC mode only
Inactive	Entered from incompatible voltage range response via Command 1 or directly from Command 15. Exited only through power cycle. MMC only.
Standby	The state where the card is "Ready" for the next command but not processing. Entered after any start bit is detected on the bus. MMC mode only.
Sleep	SanDisk's electrical, power saving mode. This mode is the lowest power mode for the MMC. It is entered automatically if no command is received within 5 msec. Exiting Sleep mode will occur automatically upon receipt of any command. Entering and exiting sleep mode is an automatic function of the card and transparent to the host.

►What is the expected Block programming time?

The time it takes to program a SanDisk memory is somewhat variable. To explain the variation one needs to understand the nature of a SanDisk memory cell. Erase and programming time for each cell may vary due to temperature, voltage and age of that cell. SanDisk's internal erase and programming controller routines are adaptive to meet and compensate for the factors described above, to ensure valid data is stored.

What SanDisk specifies is the average read/write or write/read time. This time is obviously dependent on the MMC's clock signal from the host, but, the "maximum" Write speed is ≈ 200K Bytes/sec. and 1MB/sec. at 20MHz.

The second set of values that SanDisk provides are described in the "Read, Write and Erase Time-out Conditions" section (5.4.4.2) of the SanDisk MultiMediaCard Product Manual. is total Read time for data transfer (N_{AC}). N_{AC} is the sum of TAAC (bits 119 - 112) and NSAC (bits 111 -104) of the MMC's CS register.

If TAAC = 26 hex (0010 0110 bin), then the time exponent = 6 (1mS) and the time mantissa = 2 (1.2) for a total asynchronous access time of 1.2m Sec. If NSAC = 00 hex (in hundreds of clock cycles) then the total time (N_{AC} is still TAAC + NSAC or 1.2m Sec. This time can be interpreted as a typical delay for the first data bit of a block.

The total Block programming time = N_{AC} * R2W_FACTOR (CSD bits 28 – 26). Following the existing example if R2W_FACTOR = 4 hex (100 bin), which translates to a multiple of 16 from Table 5-24. This makes the Write time = 19.2m Sec.

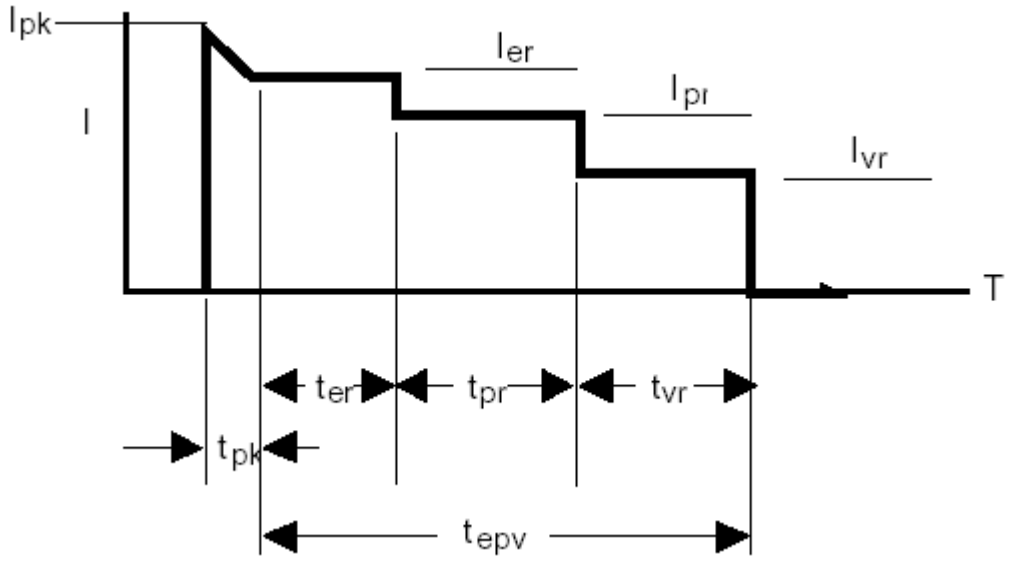
The values above are “typical” values. Worst-case timeouts can be calculated from these values by multiplying them by 10 in accordance with section 5.4.4.2 of the SanDisk MMC manual.

►What is the absolute maximum (peak) current at either a power-on cycle or a hot insertion?

The measured maximum peak current (as of 3/99) is 1.9A for 500nSec @ 2.7V and 2.1A for 500nSec @ 3.3V. This is a short current induced by the filter capacitors on the card. These currents exist for an extremely short time and are likely to improve as the product matures.

Other maximum-current values can be found in the MMC’s CSD register.

Max. Value Name	CSD bits	Symbol	Value (as of 3/99)
Read Current	58 – 56	-	35 ma
Write Current	52 – 50	-	45 ma
Peak Current	-	Ipk	< 60 ma
Erase Current	-	Ier	≈ 37 ma
Program Current	-	Ipr	≈ 35 ma
Verify Current	-	Ivr	≈ 25 ma
Peak Current Time	-	tpk	> 1µ sec
Erase Current Time	-	ter	≈ 0.5 ms
Program Current Time	-	tpr	≈ 1.5 to 3.5 ms
Verify Current Time	-	tvr	≈ 1.5 to 3.5 ms
Erase to Verify Time	-	tepv	≈ 3 to 7 ms



These values describe Read and Write currents but not the maximum power-on current.
Empirically, cards have not exceeded 60mA at power up or during hot insertion and these “peaks” have not maintained these current levels for more than ≈ 1µSec.

►What is the average or peak current draw during the 74 (or 80) initialization clock cycles?

The average is 2.5mAmps (5mAmp peak) for the first 64 clocks and then the sleep current.

►In the case of ATA products (CF and ATA), a power cycle (e.g., ramp-up time) is defined in the PCMCIA specification. Is there a similar recommended power cycle timing profile for the MMC?

The recommended power cycle timing profile is not defined in the current MMC standard, but it may be in the future. For the power supply, SanDisk uses the voltage rise time of 1.5 uSec.
Current consumption:
1.1A for 500nSec @ 3.3V
0.6A for 500nSec @ 2.7V

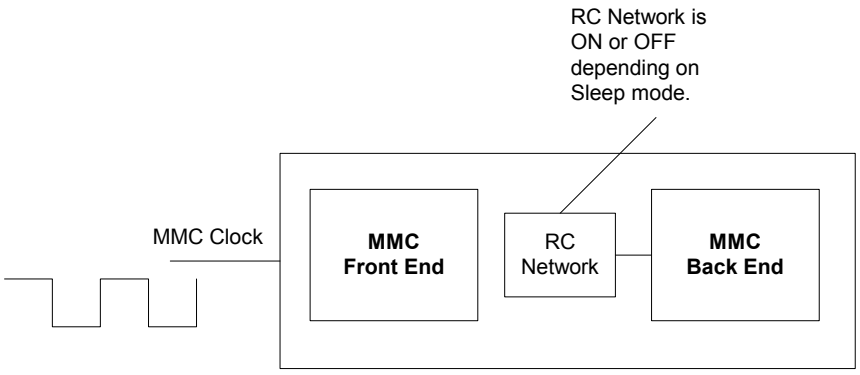
►What is the maximum ESD rating for the MMC?

At this time the absolute maximum ESD value has not been measured, but cards have been tested against the "Human Body" contact limit model. SanDisk cards meet and/or exceed the ± 4KV in accordance with MMCA spec. 1.4. All tests were taken from the Electrostatic Discharge Association's Standard Test Method for Electrostatic Discharge (ESD) Sensitivity Testing, Human Body Model (HBN) Component Level, document ESD STM5.1-1998.

►How is the Host MMC clock synchronized or related to the Internal MMC clock and can there be MMC internal operations without the External clock?

There are two functional parts to the MMC controller: the front end is controlled by the Host's clock signal to the card and an internal clock, generated via an RC network, controls the back end. These two clocks are independent of each other. The RC network clock only requires power to be applied to the card and stops during sleep mode. Both clocks are asynchronous.

Front-End functions primarily deal with the host interface and communications. Back-end functions primarily deal with internal controller register functions, flash memory communications and flash memory itself. Internal back-end functions can and do continue while the MMC Host clock is stopped.



►Can the external Host clock frequency be increased or decreased in the normal course of operation?

Yes. Clock control limits and restrictions are outlined in the *SanDisk MultiMediaCard Product Manual*. Briefly, the clock can be changed as long as the duty cycle is ≈ 50% and under 20 MHz—or rising edge to rising edge is not less than 50 ns. Exchanges are on eight clock cycle boundaries, and eight clock cycles (minimum) follow any operation.

►Why are there limiting factors for higher speed transfers in open drain mode?

Open Drain mode is necessary for a multiple MMC bus so that any card on the bus can respond without having to drive all cards. This usually means that the bus will need to run slower than the maximum speed since the rise time for the outputs are dependent on external pull-up resistors and multiple-car capacitances. Two factors may cause problems in higher speed systems.

Data transfer frequencies that are too high might begin to round or attenuate the data's rising (on falling) edges causing data miscues.
The Host might not detect slow cards. The maximum data transfer speed is a parameter of the MMC's CSD register. SanDisk cards can operate at the maximum allowable transfer rate according to the *MultiMediaCard System Specification (rev. 1.4)*. Every card on the bus may not be a SanDisk card and may have a slower maximum data transfer speed. The *MultiMediaCard System Specification (rev. 1.4)* allows any MMC to define its own maximum data transfer speed in bits 103 to 96 of the CSD up to 20 MHz.

For the SanDisk MMC, TRANS_SPEED from the CSD = 2A hex. The rate exponent (bits - 0) becomes 2 (or 10Mb/sec) and the time mantissa (bits 6 - 3) becomes 5 (or 2.0). 10Mb/s * 2.0 = 20 MHz.

As long as the host can send data at the maximum transfer rate, there are no issues for an MMC operating in SPI mode. SPI mode operates in push-pull mode only.

►What is the SPI Maximum data transfer/clock speed for SPI mode?

The maximum data transfer/clock speed is a card parameter not a protocol parameter. This means that MMC mode and SPI mode have the same maximum data transfer/clock speed of 20 MHz. The only difference is in the method used to access the data. MMC mode may have protocols, like stream mode, that are able to provide more sequential data and speed-up data access, but the clock speeds and limits are identical in both modes.

►How are bits or bytes read serially from the CSD register?

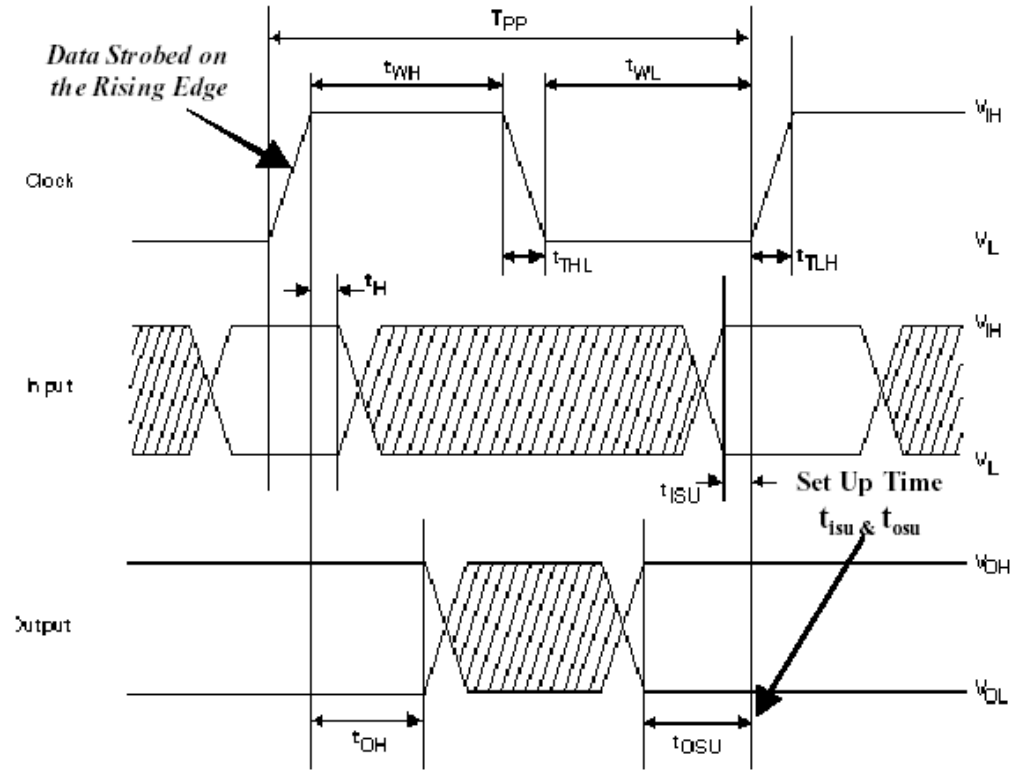
The data is read most significant bit (MSB) of the most significant byte to least significant bit (LSB) of the least significant byte. In other words, bit 127 of the CSD is shifted out first after a SEND_CSD command (CMD9) I issued. Currently, the first valid CSD bits (127 & 126), CSD_STRUCTURE, to appear for all SanDisk cards is bit 127 first as '0' followed by bit 126 as '1'.

►What is the expected (typical) gate size for both the MMC port and SPI port in the Verilog model?

The typical gate size is 8K for logic and registers (command and response FIFOs included). Data buffers are excluded.

►In reference to the *Bus Timing* section of the *SanDisk MultiMediaCard Product Manual*, where is data actually transferred?

Data is valid for both input and output on the MMC clock's rising edge. Valid data is held for minimum of 3nS (t_{IH}) for input and 5nS (t_{IH}) for output.



Note: Data in the shaded areas is not valid.

►In Stream mode (CMD20) for the MMC, how long do you wait after a Stop command (CMD12) to send the next command?

You must wait eight clock cycles.

►Will there be a lag time after a Stop command (CMD12) is issued in Stream mode (CMD20)?

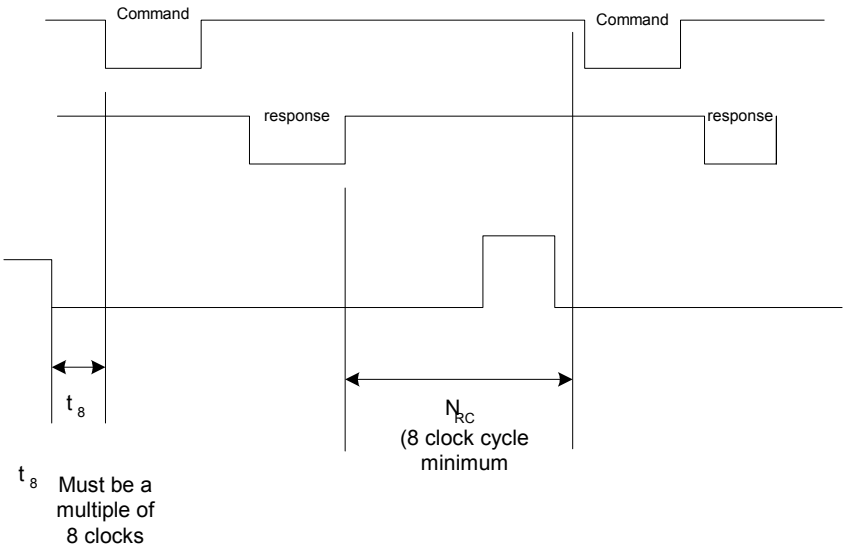
Yes, the time will be about 50 to 60 clock cycles from the time the Stop command is issued. Data transfer will stop upon detection of the Stop command.

►How much delay or how many clocks are required between SPI commands?

Eight clocks are required. This value is referred to as NRC in the Timing Constant definitions in the *MultiMediaCard Product Manual*.

►How much delay or how many clocks are required between de-assertion of the SPI, CS line to the next assertion of the CS line in SPI mode?

Zero delay is required. You can raise the CS in one cycle and assert it again the next cycle. However, there must be an eight clock delay between commands (end of response to start of command) and the start bit of a command must be byte aligned to the CS.



SanDisk Corporation
Corporate Headquarters
140 Caspian Court
Sunnyvale, CA 94089
408-542-0500 FAX: 408-542-0503
www.sandisk.com